AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (Original) A signal timing adjustment device, comprising:

a voltage generating section for generating a plurality of adjustment voltages;

a voltage selecting section for selecting, from the plurality of adjustment voltages, an adjustment voltage that is in accordance with a delay-time adjustment amount, which is set so that delay time of each circuit block in an integrated circuit becomes closer to an average value of the delay time, the delay time being time between an input of data to the circuit block and an output of the data from the circuit block; and

a delay-adjustment section for increasing or decreasing the delay time by using a transistor at which a threshold voltage changes in accordance with a value of the adjustment voltage selected.

2. (Currently Amended) ~~A~~ The signal timing adjustment device as set forth in claim 1, further comprising:

a delay measurement section for measuring the delay time.

3. (Currently Amended) ~~The~~ A signal timing adjustment device ~~as set forth in claim 2,~~ comprising:

a voltage generating section for generating a plurality of adjustment voltages;

a voltage selecting section for selecting, from the plurality of adjustment voltages, an adjustment voltage that is in accordance with a delay-time adjustment amount, which is set so that delay time of each circuit block in an integrated circuit becomes closer to an average value of the delay time, the delay time being time between an input of data to the circuit block and an output of the data from the circuit block;

a delay-adjustment section for increasing or decreasing the delay time by using a transistor at which a threshold voltage changes in accordance with a value of the adjustment voltage selected; and

a delay measurement section for measuring the delay time, wherein:

the delay measurement section includes

a pulse generating section for generating a pulse in synchronization with a high-speed clock, and shifting a generation timing of the pulse in an increment of one clock of the high-speed clock;

a latch that acquires and holds, in synchronization with a low-speed clock, data supplied from the circuit block; and

a register that acquires and holds, in synchronization with the pulse, the data supplied from the circuit block.

4. (Original) The signal timing adjustment device as set forth in claim 1, wherein:

a well of the transistor is separated from a well of another circuit that is formed on a same substrate; and

the adjustment voltage selected is applied to the well of the transistor.

5. (Original) The signal timing adjustment device as set forth in claim 1, the signal timing adjustment device being contained in the integrated circuit.

6. (Currently Amended) ~~A~~ The signal timing adjustment device as set forth in claim 5, further comprising:

a fixing section for fixing the delay-time adjustment amount.

7. (Original) A signal timing adjustment system, comprising:

a signal timing adjustment device, including

a voltage generating section for generating a plurality of adjustment voltages;

a voltage selecting section for selecting, from the plurality of adjustment voltages, an adjustment voltage that is in accordance with a delay-time adjustment amount, which is set so that delay time of each circuit block in an integrated circuit becomes closer to an average value of the delay time, the delay time being time between an input of data to the circuit block and an output of the data from the circuit block; and

a delay-adjustment section for increasing or decreasing the delay time by using a transistor at which a threshold voltage changes in accordance with a value of the adjustment voltage selected;

a delay measurement section for measuring the delay time;

an average value calculating section for calculating the average value of the delay time, the delay time having been measured by the delay measurement section; and

an adjustment amount setting section for setting the delay-time adjustment amount so that a difference between the delay time and the average value becomes smaller, the average value having been calculated by the average value calculating section.

Claim 8 (Canceled)

9. (Currently Amended) A computer-readable storage medium storing a signal timing adjustment amount setting program for a signal timing adjustment system including

a signal timing adjustment ~~device~~ section, including (i) a voltage generating section for generating a plurality of adjustment voltages, (ii) a voltage selecting section for selecting, from the plurality of adjustment voltages, an adjustment voltage that is in accordance with a delay-time adjustment amount, which is set so that delay time of each circuit block in an integrated circuit becomes closer to an average value of the delay time, the delay time being time between an input of data to the circuit block and an output of the data from the circuit block, and (iii) a delay-adjustment section for increasing or decreasing the delay time by using a transistor at which a threshold voltage changes in accordance with a value of the adjustment voltage selected;

a delay measurement section for measuring the delay time;

an average value calculating section for calculating the average value of the delay time, the delay time having been measured by the delay measurement section; and an adjustment

an adjustment amount setting section for setting the delay-time adjustment amount so that a difference between the delay time and the average value becomes smaller, the average value having been calculated by the average value calculating section,

the signal timing adjustment amount setting program causing a computer to function as the average value calculating section and the adjustment amount setting section.